REMARKS

Claims 1-23 are pending in the present application. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 103, Obviousness

A. The Examiner rejected Claims 1, 12 and 23 under 35 U.S.C. § 103 as being unpatentable over Panwar et al. (US 6,058,466). This rejection is respectfully traversed.

With respect to Claim 1, Applicants urge that the cited reference does not teach or suggest the claimed steps of (1) "determining whether a first logical processor on the first physical processor is idle", (2) "determining whether a second logical processor on the first physical processor is busy *if the first logical processor is idle*", or (3) "relinquishing resources of the first physical processor to the second logical processor *if the second logical processor is busy*". As can be seen, step (2) has two aspects – (i) determining whether a second logical processor on the first physical processor is busy, and (ii) this determining step is conditioned upon whether the first logical processor is idle. Step (3) similarly has two aspects – (i) relinquishing resources of the first physical processor to the second logical processor, and (ii) this relinquishing step is conditioned upon whether the second logical processor is busy. This is significantly different from the teachings of the cited Panwar reference for numerous reasons.

First, the cited Panwar reference does not teach any type of determination of whether a processor is busy or idle, but rather makes a determination of whether a cache miss occurs (column 7, line 67 – column 8, line 2; column 8, lines 10-13). If an on-chip cache miss occurs, *the processor is placed in a nap state* (column 7, line 67 – column 8, line 2). When a napping virtual processor (such napping virtual processor is not idle, as it continues to schedule and execute instructions – column 8, lines 6-9) encounters a cache miss that must be satisfied by main memory, the virtual processor *enters the sleep state* (column 8, lines 10-13). In both instances, *there is no determination of whether the processor is idle*, but rather *an explicit action is forced on the processor to place the processor in a given state* such as a nap state or a sleep state.

Second, the cited Panwar reference does not teach or otherwise suggest a conditional relinquishment of resources based upon whether the second logical processor is busy. Instead, the cited reference merely states that the sleeping processor is unconditionally prevented from taking additional resources and releases resources previously provided (column 8, lines 13-22). This action is not in any way based upon whether *another processor* is busy, but instead is based upon the state of *itself* (whether it encountered a cache miss). Claim 1 expressly states that resources are relinquished *if the second logical processor is busy*. The cited reference does not teach or otherwise suggest this type of conditional relinquishment of resources.

Thus, it is urged that the teachings of the cited reference are substantially different from Claim 1, in that (1) no determination is made as to whether a processor is idle or busy, but instead a processor is forced/placed into a nap or sleep state based upon a cache miss occurrence, and (2) there is no conditional relinquishment of resources that is dependent upon *whether the second logical processor is busy*. Rather, the first logical processor conditionally relinquished resources based upon a cache miss occurrence with respect to the same first logical processor. Therefore, a prima facie showing of obviousness has not been established with respect to Claim 1[1].

Applicants traverse the rejection of Claims 12 and 23 for similar reasons to those given above with respect to Claim 1.

B. The Examiner rejected Claims 2-6 and 13-17 under 35 U.S.C. § 103 as being unpatentable over Panwar et al. (US 6,058,466), in view of applicants' admitted prior art (AAPA). This rejection is initially traversed for reasons given above with respect to Claim 1. This rejection is further traversed as follows.

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[1] In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Only if that burden is met, does the burden of coming forward with evidence or argument shift to the applicant. Id. To establish prima facie obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. MPEP 2143.03 (emphasis added by Applicants). *See also, In re Royka*, 490 F.2d 580 (C.C.P.A. 1974). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In the absence of a proper *prima facie* case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Claim 2 further emphasizes the substantial differences articulated above regarding Claim 1, as Claim 2 further defines the step of determining whether the first logical processor is idle comprises (i) determining whether the first logical processor is running a current job; and (ii) determining whether a first run queue corresponding to the first logical processor is empty if the first logical processor is not running a current job, wherein the first logical processor is idle if the first run queue is empty. As can be seen, Claim 2 expressly recites two determining steps. Importantly, Claim 2 recites that the second determining step (determining whether a run queue is empty) is *conditioned upon* whether the first logical processor is not running a current job. The cited Panwar reference does not teach or suggest either of these determining steps, as it teaches that a virtual processor is placed into a particular state based upon whether a cache miss has occurred (restated, the processor state is not determined but is dictated). However, the Examiner states that this missing claimed feature is well known, citing Applicants' own Specification at page 3, lines 11-13 as evidencing this well-known feature. Applicants show two-fold error in such assertion. First, the passage cited at page 3, lines 11-13 states that 'When a logical processor becomes idle *and* there are no threads waiting in the run queue, the processor checks for threads to "steal"'. Thus, and contrary to the Examiner's assertion, this passage does not establish that it was well-known to perform a conditional determining step (determining whether a run queue is empty) which is *dependent upon whether the processor is not running a current job.* Rather, it states two independent states are determined (processor idle; no threads in run queue). Restated, this passage states a conditional action is performed (check for threads to steal) based upon two conditions being met (idle processor, no threads in run queue). This does not establish any teaching of a conditional determining of whether a run queue is empty, the condition being whether the processor is not currently running a job.

Even assuming arguendo that this passage established that it was well-known to recognized that the run queue associated with a processor is empty if the processor is not currently running a job (as alleged by the Examiner on page 4, paragraph 6 of the present office action), such "well-known" allegation is an insufficient basis for an obviousness rejection. As stated by the Federal Circuit, "virtually all [inventions] are combinations of old elements." *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 698, 218

USPQ 865, 870 (Fed. Cir. 1983); *see also Richdel, Inc. v. Sunspool Corp.*, 714 F.2d 1573, 1579-80, 219 USPQ 8, 12 (Fed. Cir. 1983) ("Most, if not all, inventions are combinations and mostly of old elements."). Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be "an illogical and inappropriate process by which to determine patentability." *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570, 38 USPQ2d 1551, 1554 (Fed. Cir. 1996). Applicants urge that since the teachings of the Panwar reference are specifically directed to reacting to a *cache miss event* to trigger associated actions, the only motivation for modifying the teachings contained therein in accordance with the invention of Claim 2 must be coming from Applicants' own patent specification and claims, which is improper hindsight analysis. When prior art references require selective combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

Still further, it would not be possible to modify the teachings of the cited Panwar reference in accordance with the claimed invention of Claim 2 and still maintain the operational characteristics provided by Panwar. Claim 2 expressly recites two distinct determining steps (current job running, run queue empty), and these two determining steps synergistically co-act to provide an overall determination of whether a processor is idle. Adding this two-fold determination to the teachings of Panwar would essentially eliminate the cache miss functionality that Panwar is keen on providing - as processor run queue status is not directly correlated with cache miss status – further evidencing no motivation to modify the Panwar teachings in accordance with the invention of Claim 2, and thus further evidencing non-obviousness of Claim 2.

Applicants traverse the rejection of Claims 3 and 4 for reasons given above with respect to Claim 2 (from which Claims 3 and 4 depend upon).

With respect to Claim 5 (and similarly for dependent Claim 6), such claim extends the methodology of Claim 1 by introducing a second physical processor having a (third) logical processor and associated run queue. In addition, Claim 5 introduces yet another conditional determination being made, in this case a determinination is made as to whether a job is available in the run queue corresponding to this third logical processor *if* the second logical processor on the first physical processor is not busy. None of the cited references contemplate such cross-processor conditional actions, where if a logical processor on one physical processor is not busy, a determination is made of whether a job is available in a run queue corresponding to a different (third) logical processor on a different (second) physical processor. In rejecting Claim 5, the Examiner states that the Panwar/AAPA combination discloses the concept of when a logical processor becomes idle and there is (sic) no threads waiting in the run queue, the processor checks for threads to acquire from another processor's run queue and that moving a thread between physical processors is expensive, and thus it is obvious to recognize that the concept of checking for threads from another processor's run queue also mean a run queue corresponding to a different physical processor as well. Applicants urge that the cited Panwar reference is directed to placing a processor into either a nap mode or a sleep mode based upon the occurrence of a cache miss. In the nap mode, the processor continues execution of resources that is has already occupied, but is not allowed to take possession of any more resources (column 8, lines 6-8). In the sleep mode, the processor is not only prevented from taking additional resources, but it is also forced to release resources previously occupied (column 8, lines 15-18). In both situations, the processor does not look for additional resources and associated work, but instead *is expressly precluded from such additional resources/work*. These are the identical passages cited by the Examiner in rejecting Claim 1 (of which Claim 5 depends upon), and hence the passages cited by the Examiner in rejecting Claim 1 in combination with Claim 5 expressly teach away from the features of Claim 5. Thus, a person of ordinary skill in the art would not have been motivated to modify the teachings of the cited references in accordance with the features of Claim 5. Although a device may be capable of being modified to run the way [the patent applicant's] apparatus is claimed, there must be a suggestion or motivation *in the reference* to do so. *In re Mills*, 916 F.2d 680, 16 USPQ2d

1430 (Fed. Cir. 1990). There is simply no reason for modifying Panwar in accordance with the features recited in Claim 5, as Panwar expressly teaches away from such features. It is thus urged that Claim 5 (and similarly for dependent Claim 6) has been erroneously rejected.

Applicants traverse the rejection of Claims 13-15 for similar reasons to those given above with respect to Claim 2.

Applicants traverse the rejection of Claims 16 and 17 for similar reasons to those given above with respect to Claim 5.

C. The Examiner rejected Claims 7, 8 and 18-19 under 35 U.S.C. § 103 as being unpatentable over Panwar et al. (US 6,058,466), in view of AAPA, and further in view of Koning (US Pat. Application Publication 2002/0133530). This rejection is initially traversed for reasons given above with respect to Claim 1. This rejection is further traversed as follows.

Claim 8 recites an explicit step of *lowering the priority* of the first logical processor as a part of the step of relinquishing resources (recited in Claim 1). In rejecting Claim 8, the Examiner cites Koning's teaching of a scheduler at page 7, paragraph 0087 as evidencing this claimed feature as being obvious. Applicants urge that Koning's scheduler is not in any way involved with changing or modifying priorities of tasks. Rather, it is a traditional, unmodified scheduler that merely schedules tasks *based upon their existing priorities*. Therefore, the Examiner has failed to properly establish a prima facie showing of obviousness with respect to Claim 8, as none of the cited references teach or otherwise suggest the claimed step of *lowering a priority* of a first logical processor in order to relinquish resources of the first physical processor to the second logical processor if the second logical processor is busy. Applicants respectfully submit that since Koning merely teaches use of a traditional scheduler using preexisting priorities, the Examiner has failed to establish any teaching or suggestion of the features recited in Claim 8, and thus a proper prima facie showing of obviousness has not been established, and therefore Claim 8 has been erroneously rejected.

Applicants further traverse the rejection of Claim 19 for similar reasons to those given above with respect to Claim 8.

D. The Examiner rejected Claims 9 and 20 under 35 U.S.C. § 103 as being unpatentable over Panwar et al. (US 6,058,466), in view of AAPA, in view of Koning (US Pat. Application Publication 2002/0133530), and further in view of Welland et al. (US 5,247,677). This rejection is traversed for reasons given above with respect to Claim 8.

E. The Examiner rejected Claims 10, 11, 21 and 22 under 35 U.S.C. § 103 as being unpatentable over Panwar et al. (US 6,058,466), in view of AAPA, in view of Koning (US Pat. Application Publication 2002/0133530), in view of Welland et al. (US 5,247,677), and further in view of Kimmel et al. (US 6,105,053). This rejection is traversed for reasons given above with respect to Claim 9.

In conclusion, it is urged that the primary Panwar reference is directed to techniques for managing cache misses and restricting further processor activity in response thereto, and thus there would have been no motivation to modify the Panwar teachings in accordance with the features recited in Claims 1-22 as such modification would eviscerate the expressed purpose of the Panwar teachings.

Therefore, the rejection of Claims 1-22 under 35 U.S.C. § 103 has been overcome for all the reasons described above.

II. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 6/1/05

Respectfully submitted,

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